

An advancement in the $N \times N$ Multiplier Architecture Realization via the Ancient Indian Vedic Mathematics

Neeraj Mishra, Asmita Haveliya

Abstract – Multiplication is an crucial unfussy, basic function in arithmetic procedures and Vedic mathematics is a endowment prearranged for the paramount of human race, due to the capability it bestows for quicker intellectual computation. This paper presents the effectiveness of Urdhva Triyagbhyam Vedic technique for multiplication which cuffs a distinction in the authentic actual development of multiplication itself. It facilitates parallel generation of partial products and eradicates surplus, preventable multiplication steps. The anticipated $N \times N$ Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using Xilinx ISE Design Suite 13.1. The projected architecture is a $N \times N$ Vedic multiplier whilst the VHDL coding is done for 128×128 bit multiplication process. The result shows the efficiency in terms of area employment and rapidity.

Keywords – Vedic Multiplier, Urdhva-Triyagbhyam Sutra, $N \times N$ Vedic Multiplier, Vedic Multiplication Process.

I. INTRODUCTION

Vedic mathematics is a quality inheritance given to the humankind by the ancient sages of India. It is the name given to the ancient system of mathematics, which was restructured from ancient Vedic texts of Atharva Veda early in the last century by Sri Bharati Krishna Tirthaji . It is based on a set of 16 sutras (or aphorisms) dealing with mathematics linked with arithmetic, algebra, and geometry. These modus operandi and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of different kinds. The sophistication of Vedic mathematics lies in the fact that it moderates otherwise burdensome cumbersome looking calculations in conventional mathematics to a much uncomplicated ones. It is for the reason that the Vedic formulae are claimed to be based on the ordinary ideology on which the individual's intelligence works. This is a stimulating and exhilarating field and illustrates some efficient clichés which can be applied to different branches of engineering such as computing and digital signal processing. In the projected work we are using the urdhva-triyagbhyam sutra of the ancient Indian Vedic mathematics, this aphorism of the grand ancient Indian Vedic mathematics requires no elucidation and enlightenment, for that reason we are not amplifying this algorithm in the manuscript, even though how the sutra is placed into maneuver in our work, is a matter of justification and is elucidated in the proposed multiplier architecture segment.

The paper is organized as follows. Section II illustrates the proposed multiplier architecture based on Vedic multiplication and the generalized indiscriminate algorithm for $N \times N$ bit Vedic multiplier. Section III

describes the design and implementation of Vedic multiplier module implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language), furthermore the FPGA and CPLD synthesis with the discussion of device utilization summary and computational path delay obtained for the proposed Vedic multiplier (after synthesis) is also illustrated in this section using Xilinx ISE Design Suite 13.11.

II. PROPOSED MULTIPLIER ARCHITECTURE

The traditional mathematics is a fundamentally indispensable fraction of engineering edification, since the prevalent component of engineering structure is supported within the reach of assorted mathematical approaches. A multiplier is one of the central hardware blocks in the major part of digital signal processing systems. With evolution in the advancement in technology, numerous researchers are making a tremendous effort to design multipliers which tender whichever of the subsequent-high speed, low power utilization, regularity of layout and hence less area or even grouping of them in multiplier. The gate level realization of the projected work for two bit number as obtained by the Xilinx ISE Design Suite 13.1 using the concept of the *Urdhva-Tiryagbhyam* sutra of the ancient Indian Vedic mathematics is shown in figure 1, while the actual gate level realization utilized in the proposed work is shown in figure 2 .

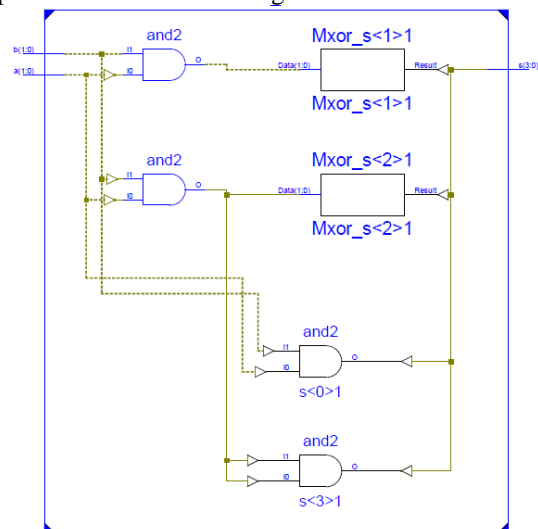


Fig.1. Gate level realization of the projected work for two bit multiplier

Subsequent to the realization and implementation of the two bit multiplication component, somewhat comparable progression is accumulated in the design organization of the four bit multiplication architecture and so on. The diminutive but the significant difference being, instead of

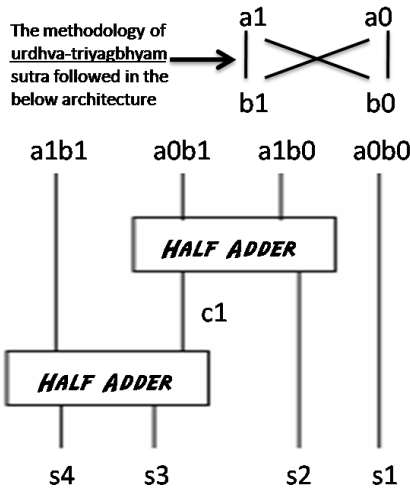
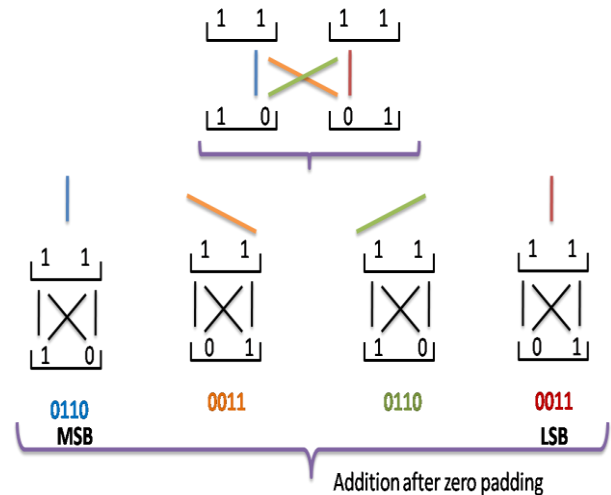


Fig.2. Gate level realization utilized in the proposed work for two bit multiplier

using the multiple adder modules we are here using a technique of zero padding and then as a final point an adder module. Consider, if we are talking about $N \times N$ bit multiplier module then we will have to use four $\frac{N}{2} \times \frac{N}{2}$ bit multiplier modules. Let's acquire an illustration model of a four bit multiplier module for the enlightenment on the projected work.

Consider the first four bit number: 1 1 1 1
 And now the second four bit number: 1 0 1 0

As mentioned 4×4 multiplier requires four modules of 2×2 multipliers. So these four bits numbers are multiplied with the approach exemplified using the diagrammatical illustration in figure 3.



0	1	1	0	0	0	0	0	MSB
0	0	0	0	0	0	1	1	LSB
0	0	0	0	1	1	0	0	
0	0	0	1	1	0	0	0	
1	0	0	0	0	1	1	1	

Fig.3. The diagrammatical illustration for the proposed architecture

Now the whole development structure followed for the 4×4 multiplier is shown in the figure 4.

Following the extremely comparable analogous approach we are proposing a $N \times N$ bit multiplier. The main projected structure for the $N \times N$ bit multiplier is anticipated in figure 5.

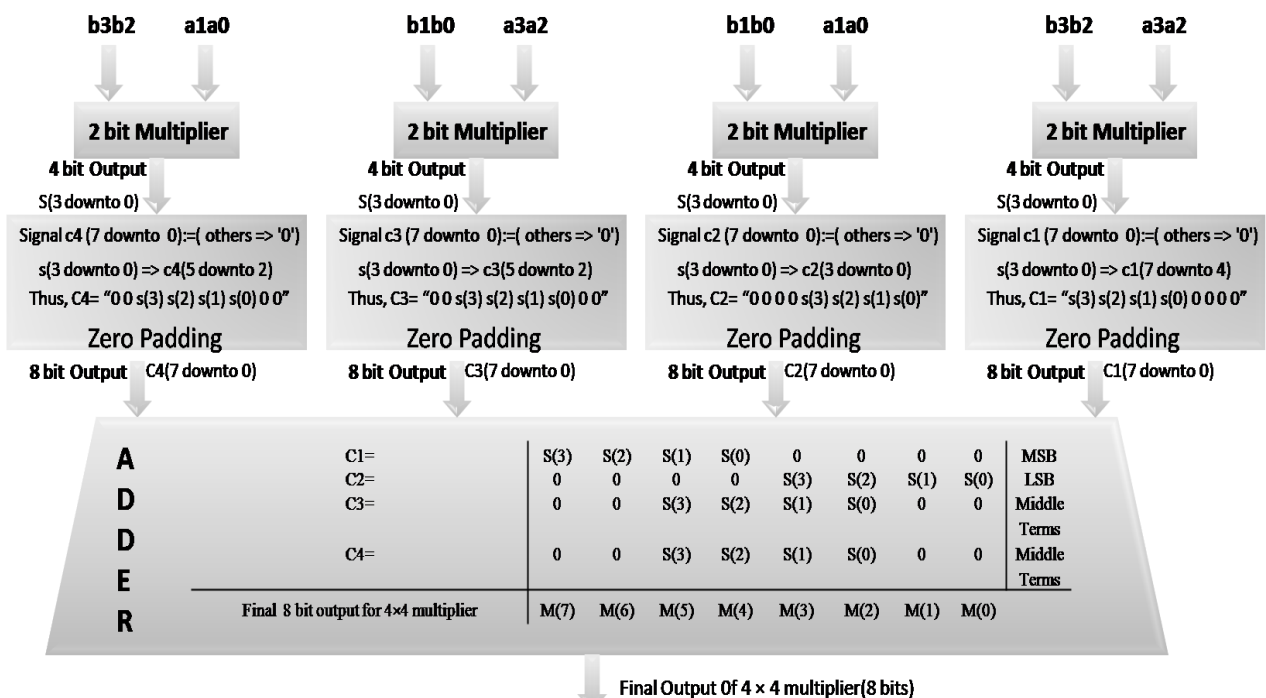


Fig.4. The proposed architecture for four bit multiplier

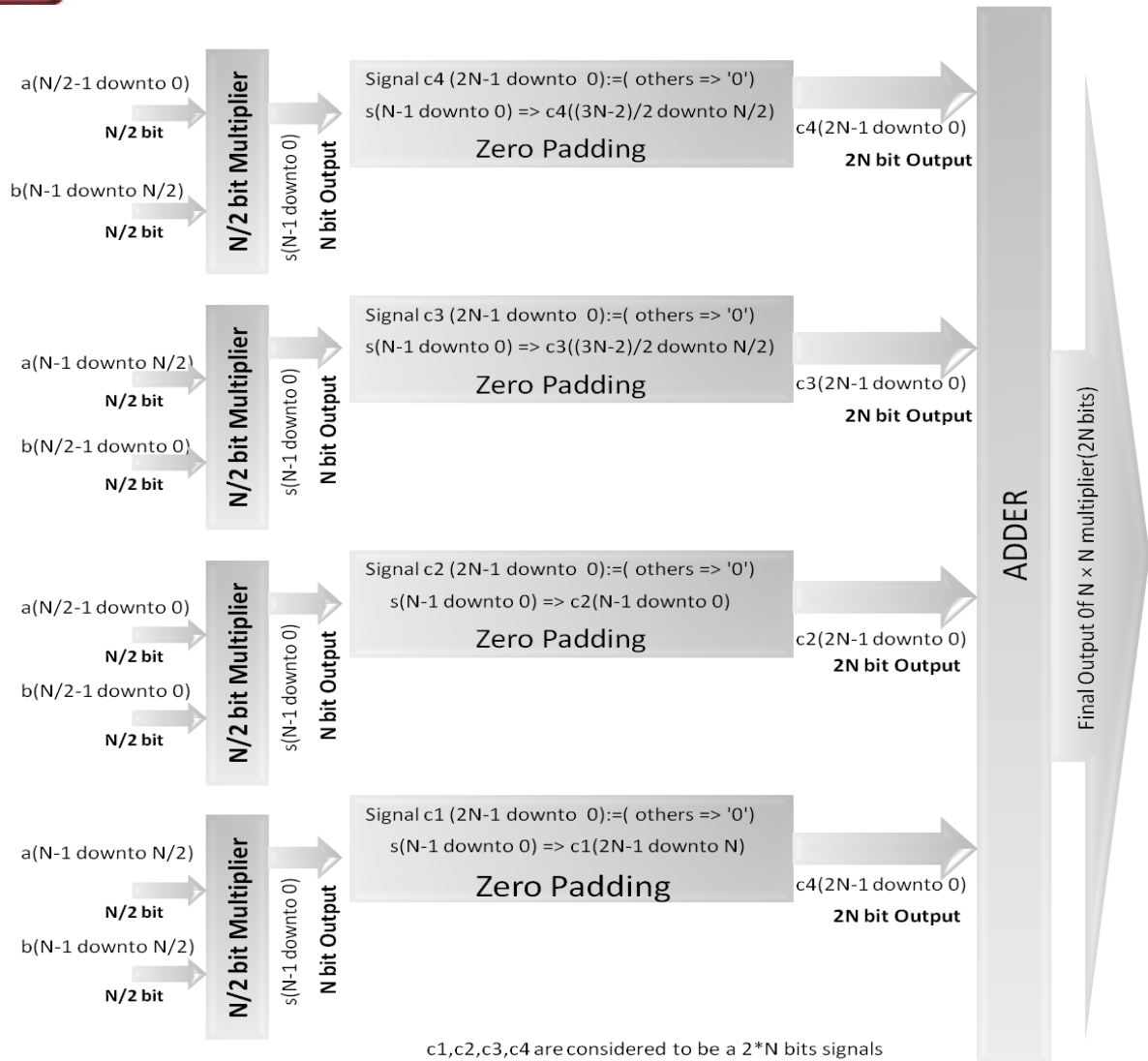


Fig.5. The proposed architecture for $N \times N$ bit multiplier

III. RESULT

The proposed multiplier architecture is implemented in VHDL (Very High Speed Integrated Circuited Hardware Description Language) furthermore the FPGA and CPLD synthesis is done using Xilinx ISE Design Suite 13.1. The design is optimized for speed and area using Xilinx, in the midst of the subsequent device families.

- [1] Virtex 7 XC7V2000T, package FFG1925, speed grade -1.
- [2] Virtex 7 XC7V285T, package FFG1157, speed grade -1.
- [3] Virtex 7 XC7V285T, package FFG1157, speed grade -3.
- [4] Virtex 7 low power XC7V285TL, package FFG1925, speed grade -1L.
- [5] Virtex 7 low power XC7V2000TL, package FFG1925, speed grade -1L.
- [6] Virtex 6 low power XC6VLX75TL, package FF484, speed grade -1L.
- [7] Spartan 6 low power XC6SLX4L, package TQG144, speed grade -1L.

[8] Kintex 7 low power XC7K30TL, package FBG484, speed grade -1L.

[9] CoolRunner-II CPLDs Automatic XC2C000.

For the implementation methodology, proposed Multipliers have been demonstrated and compared to endow with confirmation to facilitate that the projected effort is splendidly efficient in terms of the area utilization, in the TABLE I underneath. These logic utilizations are confirmed for the 128×128 bit Multiplier module using the proposed structure of $N \times N$ multiplier as illustrated in figure 5.

The Xilinx Virtex 7 low power XC7V285TL, package FFG1925, speed grade -1L, device is found to be the most efficient in terms of both speed and area as demonstrated in TABLE 1, the device contains 1221600 slices and 51030 input Look Up Tables and 1200 bonded Input/output pads. The delay for the proposed work with this particular device is:

23.493ns (11.499ns logic, 11.994ns route)
(48.9% logic, 51.1% route)

Table 1: Synthesis report for 128 × 128 bit multiplier for a fusion of devices

	Family	Device	Package	Speed	Logic Utilization	Used	Available	Utilization
F P G A	Virtex 7	XC7V2000T	FFG1925	-1	Number of Slice LUTs	51030	1221600	4%
					Number of fully used LUT-FF pairs	0	51030	0%
	Virtex 7 low power	XC7V2000TL	FFG1925	-1L	Number of bonded IOBs	512	1200	42%
					Number of Slice LUTs	51030	178800	28%
	Virtex 7	XC7V285T	FFG1157	-1	Number of fully used LUT-FF pairs	0	51030	0%
					XC7V285T	FFG1157	-3	Number of bonded IOBs
	Virtex 6 low power	XC6VLX75TL	FF484	-1L				Number of Slice LUTs
					Number of fully used LUT-FF pairs	0	51030	0%
					Number of bonded IOBs	512	240	213%
	Spartan 6 low power	XC6SLX4L	TQG144	-1L	Number of Slice LUTs	51030	2400	2126%
					Number of fully used LUT-FF pairs	0	51030	0%
					Number of bonded IOBs	512	102	501%
	Kintex 7 low power	XC7K30TL	FBG484	-1L	Number of Slice LUTs	51030	19000	268%
					Number of fully used LUT-FF pairs	0	51030	0%
					Number of bonded IOBs	512	150	341%
C P L D	CoolRunner-II CPLDs	Automatic XC2C000	NA	NA	Number of Slice LUTs	NA	NA	NA
					Number of fully used LUT-FF pairs	NA	NA	NA
					Number of bonded IOBs	NA	NA	NA

The synthesis report obtained in Xilinx ISE Design Suite 13.1 shows the Advanced HDL Synthesis Report for the Xilinx Virtex 7 low power XC7V285TL, package FFG1925, speed grade -1L (Table III) while for the Xilinx CoolRunner-II CPLDs Automatic XC2C000 the report is shown in Table II

Table II. Macro Statistics for CPLD

# Adders/ Subtractors	4095
128-bit adder	12
16-bit adder	768
256-bit adder	3
32-bit adder	192
64-bit adder	48
8-bit adder	3072

Table III. Macro Statistics for FPGA

# Adders/ Subtractors	63
128-bit adder	12
256-bit adder	3
64-bit adder	48
# Adder Trees	1344
16-bit / 4-inputs adder tree	256
32-bit / 4-inputs adder tree	64
8-bit / 4-inputs adder tree	1024
# Xors	8192
1-bit xor2	8192

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